AMENDMENT

Please amend the claims as follows:

1. (Currently amended) A dual damascene method of forming an interconnect structure of a semiconductor device, the interconnect structure having a dielectric material deposited over an underlying interconnect layer and having a via extending through the dielectric material for establishing a connection between an underlying conductor and a trench in an upper portion of the dielectric material, comprising the steps of:

(a) forming a mask layer over the dielectric material;

(b) etching the mask layer to a predetermined depth forming a via in the mask layer ~~to a first predetermined depth of the mask layer~~ without exposing the underlying dielectric material;

(c) then etching the mask layer to a second predetermined depth of the mask layer less than the first predetermined depth forming a trench in the mask layer;

(d) forming a via through the dielectric material to the underlying conductor, corresponding to the dimensions of the via formed in the mask layer; and,

(e) forming a trench in the dielectric material to a predetermined depth of the dielectric material corresponding to the dimensions of the trench formed in the mask layer.

2. (Original) The method of claim 1 further including the step of removing a predetermined amount of the mask layer from the semiconductor device and leaving a film of the mask layer thereon over the dielectric material.

3. (Original) The method of claim 1 wherein said dielectric material includes a via dielectric layer formed over the interconnect layer, a barrier layer disposed between the via dielectric layer and the interconnect layer, a trench dielectric layer formed over the via dielectric layer, and an etch stop layer disposed between the trench dielectric layer and the via dielectric layer.

4. (Currently amended) The method of claim 3 wherein said step of ~~etching~~ forming the via includes etching the via through the via dielectric layer and the barrier layer, and the step of etching the trench includes etching the trench through the trench dielectric layer.

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5. (Original) The method of claim 4 further including the step of removing a predetermined amount of the mask layer from the semiconductor device and leaving a film of the mask layer thereon over the dielectric material.

6. (Currently amended) A dual damascene method of forming an interconnect structure using a mask layer deposited over a dielectric material which has been deposited over an underlying interconnect layer, comprising the steps of:

(a) forming a first mask film over the dielectric material having a known set of etch properties;

(b) forming a second mask film over the first mask film having a known set of etch properties different from the etch properties of the first mask film;

(c) forming a third mask film over the second mask film having etch properties substantially identical to the etch properties of the first film; and,

(d) forming a fourth mask film over the third mask film having etch properties substantially identical to the etch properties ~~to the etch properties~~ of the second mask film; ~~and~~

(e) ~~selectively etching the mask films in multiple steps to form the interconnect structure~~ etching the mask films to form a via within the mask layer to a first predetermined depth and down to the first mask film without exposing the underlying dielectric layer; and

(f) then selectively etching the mask films to form a trench within the mask layer to a second predetermined depth less than the first predetermined depth of the mask layer previously etched in the mask layer.

7. (Original) The method of claim 6 further including the steps of forming a via through the dielectric material to the underlying interconnect layer and forming a trench within the dielectric material, to a predetermined depth of the dielectric material.

A1 cont.

8. (Currently amended) The method of claim 6 further including the steps of etching a portion of the first mask film to form ~~forming~~ the via in the mask layer [down to the first mask film] exposing the underlying dielectric material and etching the third mask film to form ~~forming~~ the trench in the mask layer down to the ~~third~~ second mask film.

9. (Original) The method of claim 8 further including the steps of forming the via through the dielectric material and forming the trench to a predetermined depth of the dielectric material.

10. (Currently amended) The method of claim 8 further including the steps of forming a via through the dielectric material, and ~~forming a trench in the mask layer down to the first mask layer and~~ forming a trench in the dielectric material to a predetermined depth of the dielectric material after forming a trench in the mask layer down to the first mask layer.

11. (Original) The method of claim 10 further including the step of removing the third and fourth mask films from the semiconductor device.

12. (Original) The method of claim 10 further including the step of removing the second mask film, the third mask film and the fourth mask film from the semiconductor device.

13. (Original) The method of claim 8 further including the steps of forming a via dielectric layer over the underlying interconnect layer, forming a trench dielectric layer over the via dielectric layer, forming an etch stop layer between the via dielectric layer and trench dielectric layer.

14. (Currently amended) The method of claim 13 the steps of ~~simultaneously forming the via through~~ etching the via in the trench dielectric layer in accordance with dimensions of the via formed in the mask layer, then simultaneously etching the etch stop layer in accordance with the dimensions of the via and etching the fourth mask film from the semiconductor device.

A1 cont.

15. (Original) The method of claim 8 further including the steps forming a barrier layer between the via dielectric layer and the interconnect layer.

16. (Currently amended) The method of claim 15 the steps of ~~simultaneously forming the via through~~ etching the via in the via dielectric layer to the barrier layer, and in accordance with dimensions of the via formed in the mask layer, then simultaneously etching the barrier layer and removing the third mask film from the semiconductor device.

17. (Currently amended) The method of claim 16 further including the steps of forming the trench ~~through~~ in the trench dielectric layer, and simultaneously forming the via in the via dielectric layer before etching the barrier layer [removing the etch stop layer exposed within the trench and the second mask film].

18. (Currently amended) A dual damascene method of forming an interconnect structure using a mask layer deposited over a dielectric material which has been deposited over an underlying interconnect layer, comprising the steps of:

(a) forming a via dielectric layer over the underlying interconnect layer,

(b) forming a trench dielectric layer over the via dielectric layer,

(c) forming an etch stop layer between the via dielectric layer and trench dielectric layer;

(d) forming a barrier layer between the via dielectric layer and the interconnect layer;

(e) forming a first mask film over the dielectric material having a known set of etch properties;

(f) forming a second mask film over the first mask film having a known set of etch properties different from the etch properties of the first mask film;

~~(g)~~ forming a third mask film over the second mask film having etch properties substantially identical to the etch properties of the first film; ~~and~~

A1 cont

(h) forming a fourth mask film over the third mask film having etch properties substantially identical to the etch properties to the etch properties of the second mask film~~.~~; and

(i) etching the mask films to a first predetermined depth of the mask layer without exposing the underlying dielectric and to form a via within the mask layer; and

(j) then etching the mask films to a second predetermined depth of the mask layer which is less than the first predetermined depth previously etched in the mask layer to form a trench within the mask layer.

19. (Currently amended) The method of claim 18 further including the steps of forming a via in the mask layer down to the first mask film and then forming a trench in the mask layer down to the third mask film, and the trench overlapping the via.

20. (Original) The method of claim 19 further including the steps of forming a via through the dielectric layer and the barrier layer corresponding to the dimensions of the via formed in the mask layer, forming a trench through the trench dielectric layer corresponding to the dimensions of the trench formed in the mask layer, and said trench in the trench dielectric overlapping the via in the via dielectric layer.

21. (Original) The method of claim 20 further including the step of removing the fourth mask film and the third mask film from the semiconductor device.

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22. (Original) The method of claim 21 further including the step of removing the second mask film.